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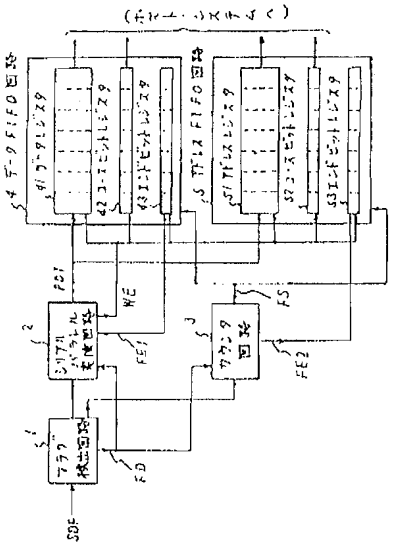
TITLE : DATA RECEPTION CONTROL CIRCUIT



ABSTRACT : PURPOSE: To receive and process continuously transmitted frames without having an influence upon the processing speed of a host system neither losing them by storing an address field, a control field, and an information field in FIFO circuits independent of one another respectively to process them.

CONSTITUTION: Serial reception data SDT transmitted from a flag detecting circuit 1 is assembled to parallel reception data PDT by a serial/parallel converting circuit 2 and the data is outputted. A counter circuit 3 is a detecting and selecting means and starts counting of reception data by a flag detection signal FD and selects the write destination of parallel reception data RDT in accordance with the counted value. That is, in the case of the HDLC protocol, first and second bytes are regarded as data of the address field and the control field to select an address FIFO circuit 5, and third and following bytes are regarded as data of the information field to select a data FIFO circuit 4. Each time of assembling, parallel reception data PDT is transferred to an address register 51 or a data register 41 by a write signal WE and a FIFO select signal FS.